

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING - AI & ML

Lesson Plan & Work done Diary for AY: 2026-27 Odd Semester

Course with Code: DIGITAL DESIGN AND COMPUTER ORGANIZATION- 1BCS303					Faculty: Dr. Uma Mahesh R N		Semester & Section: 3 RD 'A'	
Module	Class No.	Date planned (DD/MM)	Topics to be covered	TLP Planned	Date of Conduction (DD/MCS)	Topics Covered	TLP Executed	Remarks if any deviation
MODULE-1	1		Boolean Algebra and Logic Gates: Basic Theorems And Properties of Boolean Algebra.	PPT + Chalk & Board				
	2		Basic Theorems And Properties of Boolean Algebra.	PPT + Chalk & Board				
	3		Boolean Functions	PPT + Chalk & Board				
	4		Boolean Functions	PPT + Chalk & Board				
	5		Digital Logic Gates	PPT + Chalk & Board				
	6		Integrated Circuits.	PPT + Chalk & Board				
	7		Gate-Level Minimization: Introduction	PPT + Chalk & Board				

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	8		The Map Method	PPT + Chalk & Board				
	9		Four-Variable K-Map	PPT + Chalk & Board				
	10		Product of sums simplification	PPT + Chalk & Board				
	11		Don't-Care Conditions	PPT + Chalk & Board				
	12		NAND and NOR Implementation.	PPT + Chalk & Board				

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MODULE-2	13		Combinational Logic: Introduction	PPT + Chalk & Board				
	14		Combinational Circuits, Analysis of Combinational Circuits, Design Procedure, Binary Adder	PPT + Chalk & Board				
	15		Binary Subtractor	PPT + Chalk & Board				
	16		Decoders, Encoders	PPT + Chalk & Board				
	17		Multiplexers	PPT + Chalk & Board				
	18		Multiplexers	PPT + Chalk & Board				
	19		Synchronous Sequential Logic: Introduction, Sequential Circuits	PPT + Chalk & Board				
	20		Sequential Circuits	PPT + Chalk & Board				
	21		Storage Elements: Latches	PPT + Chalk & Board				

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MODU LE-2	22		Storage Elements: Latches	PPT + Chalk & Board				
	23		Flip-Flops	PPT + Chalk & Board				
	24		Flip-Flops	PPT + Chalk & Board				

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Module	Class No.	Date planned (DD/MM)	Topics to be covered	TLP Planned	Date of Conduction (DD/MM)	Topics Covered	TLP Executed	Remarks if any deviation
MODULE-3	25		Basic Structure of Computers: Functional Units	PPT + Chalk & Board				
	26		Basic Operational Concepts	PPT + Chalk & Board				
	27		Bus structure	PPT + Chalk & Board				
	28		Performance – Processor Clock, Basic Performance Equation, Clock Rate	PPT + Chalk & Board				
	29		Instruction Set: CISC an RISC, Performance Measurement	PPT + Chalk & Board				

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	30		Machine Instructions and Programs: Memory Location and Addresses	PPT + Chalk & Board				
	31		Memory Operations	PPT + Chalk & Board				
	32		Memory Operations	PPT + Chalk & Board				
	33		Instruction and sequencing, Modes.	Instruction Addressing	PPT + Chalk & Board			
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MO DUL E-4	35		Input/Output Organization: Accessing I/O Devices	PPT + Chalk & Board				

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MOD ULE- 4	36		Interrupts – Interrupt Hardware	PPT + Chalk & Board				
	37		Enabling and Disabling Interrupts	PPT + Chalk & Board				
	38		Handling Multiple Devices	PPT + Chalk & Board				
	39		Handling Multiple Devices	PPT + Chalk & Board				
	40		Direct Memory Access, Buses	PPT + Chalk & Board				
	41		The Memory System: Some Basic Concepts	PPT + Chalk & Board				
	42		Semiconductor RAM Memories	PPT + Chalk & Board				
	43		Read Only Memory	PPT + Chalk & Board				
	44		Speed, size and Cost of memory systems	PPT + Chalk & Board				
	45		Speed, size and Cost of memory systems	PPT + Chalk & Board				
	46		Cache Memories – Mapping Functions	PPT + Chalk & Board				

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Module	Class No.	Date planned (DD/MM)	Topics to be covered	TLP Planned	Date of Conduction (DD/MM)	Topics Covered	TLP Executed	Remarks if any deviation	
MODULE-5	47		Basic Processing Unit: Some Fundamental Concepts	PPT + Chalk & Board					
	48		Execution of a Complete Instruction	PPT + Chalk & Board					
	49		Execution of a Complete Instruction	PPT + Chalk & Board					
	50		Multiple Bus Organization	PPT + Chalk & Board					
	51		Multiple Bus Organization	PPT + Chalk & Board					
	52		Hardwired Control	PPT + Chalk & Board					
	53		Pipelining: Basic concepts	PPT + Chalk & Board					
	54		Role of Cache memory	PPT + Chalk & Board					
	55		Role of Cache memory	PPT + Chalk & Board					
	56		Pipeline Performance	PPT + Chalk & Board					

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Practical Component	Class No.	Date planned (DD/MM)	Topics to be covered	TLP Planned	Date of Conduction (DD/MM)	Topics Covered	TLP Executed	Remarks if any deviation
Experiments	1		Simplify a given 4-variable Boolean expression using appropriate minimization techniques and implement the simplified function using basic logic gates through simulation.	PPT + Chalk & Board				
	2		Design and simulate a 4-bit adder-Subtractor circuit using basic logic gates, and verify its functionality for different input combinations.	PPT + Chalk & Board				
	3		Design Verilog HDL to implement Binary Adder-Subtractor – Half and Full Adder, Half and Full Subtractor.	PPT + Chalk & Board				
	4		Design Verilog program to implement types of De-Multiplexer.	PPT + Chalk & Board				
	5		Design Verilog program for implementing various types of Flip-Flops such as SR, JK and D.	PPT + Chalk & Board				
	6		Design and implement Verilog programs for SR and JK Flip-Flops. Verify their functionality using simulation.	PPT + Chalk & Board				

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Practical Component	Class No.	Date planned (DD/MM)	Topics to be covered	TLP Planned	Date of Conduction (DD/MM)	Topics Covered	TLP Executed	Remarks if any deviation
Experiments	7		Identify and document the processor type, clock speed, cache memory, RAM capacity, storage devices, and operating system details of a desktop computer using system information tools.	PPT + Chalk & Board				
	8		Observe and record CPU utilization, memory usage, disk activity, and running processes using Task Manager/System Monitor before and after executing multiple applications, and compare the changes in system resource usage.	PPT + Chalk & Board				
	9		Measure file transfer rates and access times using desktop computers and discuss their impact on overall system performance and memory hierarchy.	PPT + Chalk & Board				
	10		Compare the features, instruction formats, and performance characteristics of CISC and RISC architectures through the study of modern processors, and summarize the findings in a comparative table.	PPT + Chalk & Board				
	11		Study of semiconductor RAM and ROM organization with practical examples by determining memory capacity, address lines, data lines, and memory locations, and compare their characteristics.	PPT + Chalk & Board				

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12	Identify the major hardware components of a computer system through hands-on inspection, and demonstrate the ability to safely disassemble and reassemble the system while maintaining its functionality.	PPT + Chalk & Board							
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	Activity	Planned	Actual	Remarks
1	Theory Classes + Practical Classes	56 hrs Theory + 12 hrs Lab		
2	Assignments/ Quizzes/ Self-study	2 Assignments		
3	Tutorials/ Extra classes	0		
4	Internal Assessments	3 + 1 Improvement IA		
5	ICT based Teaching (% of usage in Curriculum)	100%		
Planning			Execution	
Faculty Signature:			Faculty Signature:	
HoD Signature:			HoD Signature:	



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